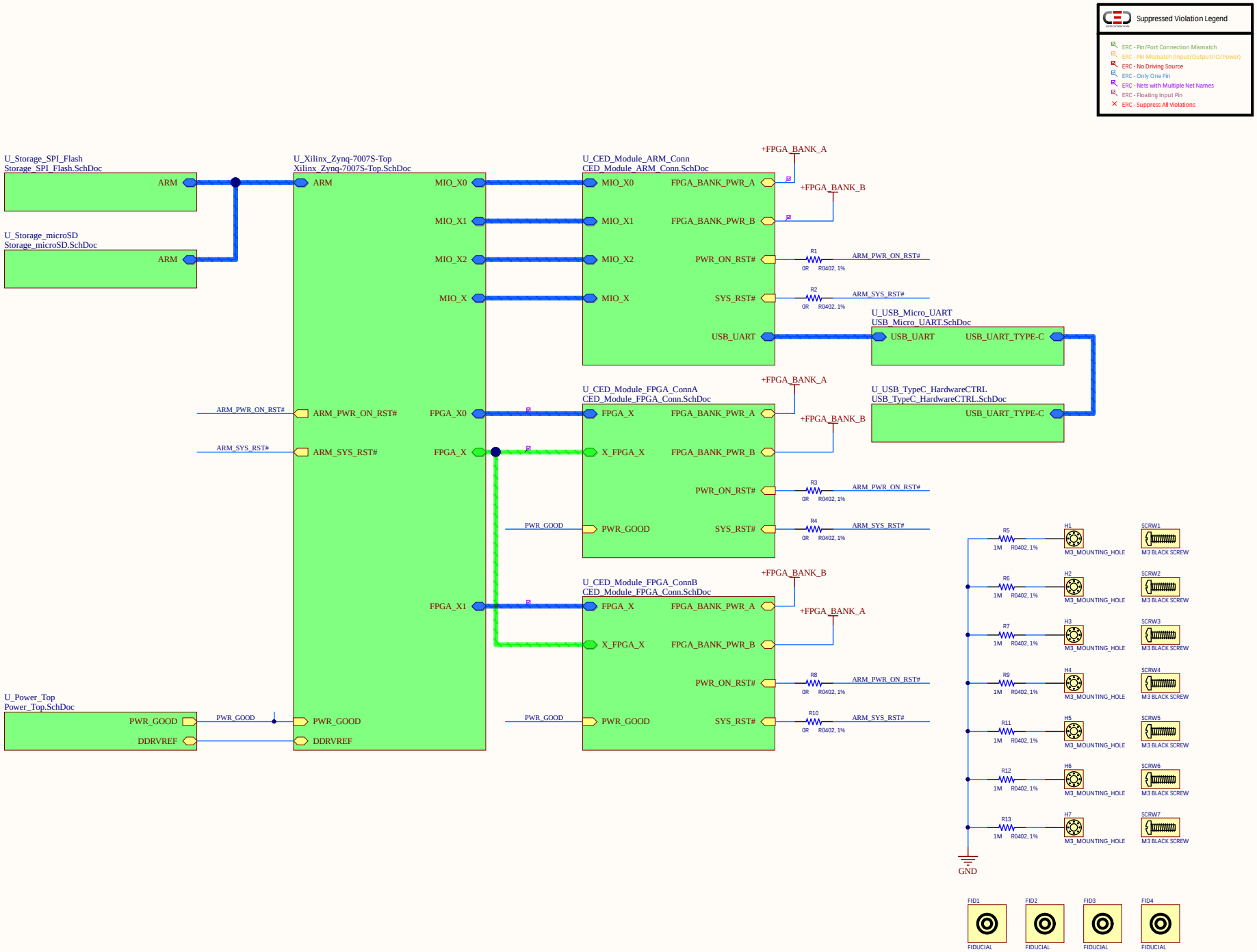
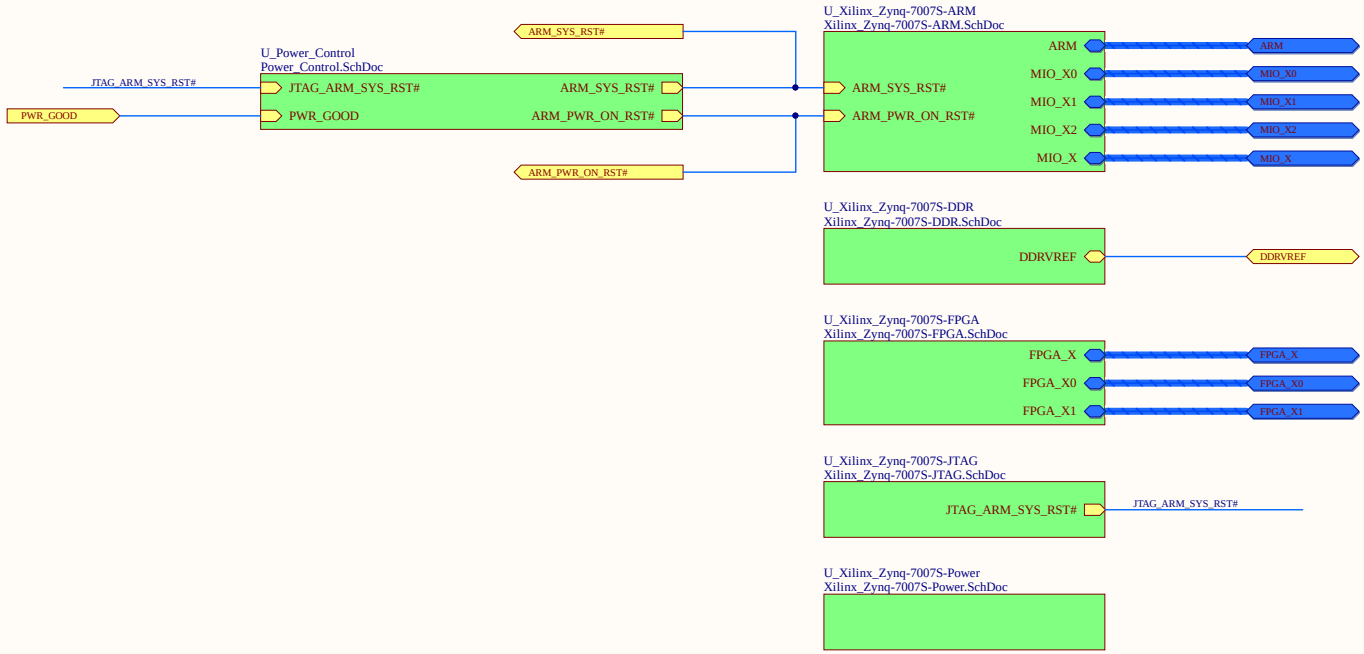
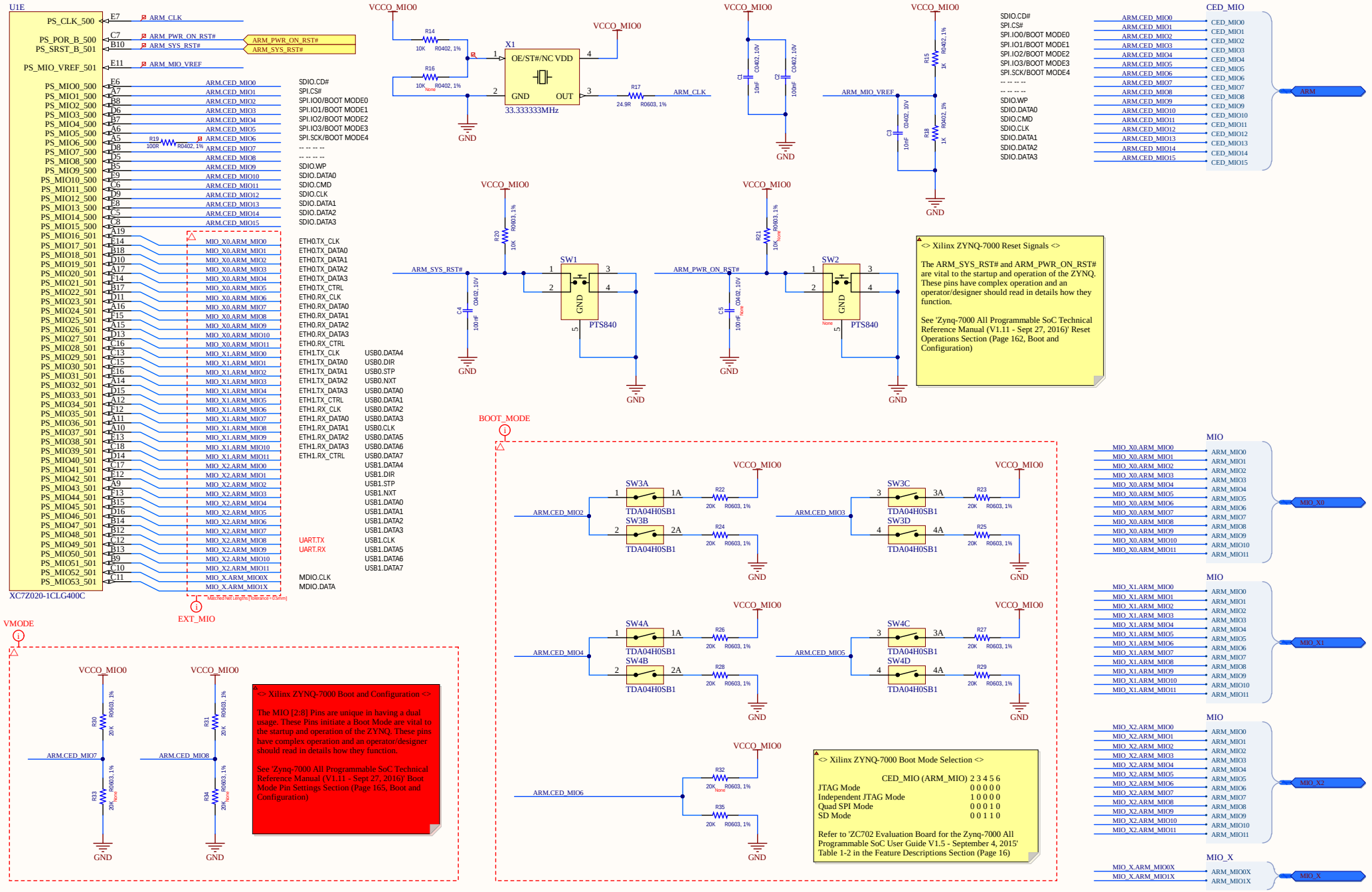

Suppressed Violation Legend
ERC - Pin/Port Connection Mismatch
ERC - Pin Mismatch (Input/Output/IO/Power)
ERC - No Driving Source
ERC - Only One Pin
ERC - Nets with Multiple Net Names
ERC - Floating Input Pin
ERC - Suppress All Violations
U_Storage_SPI_Flash
Storage_SPI_Flash.SchDoc
ARM
U_Storage_microSD
Storage_microSD.SchDoc
ARM
U_Xilinx_Zynq-7007S-Top
Xilinx_Zynq-7007S-Top.SchDoc
ARM
MIO_X0
MIO_X1
MIO_X2
MIO_X
ARM_PWR_ON_RST#
ARM_SYS_RST#
FPGA_X0
FPGA_X
FPGA_X1
PWR_GOOD
DDRVREF
U_CED_Module_ARM_Conn
CED_Module_ARM_Conn.SchDoc
MIO_X0
MIO_X1
MIO_X2
MIO_X
USB_UART
FPGA_BANK_PWR_A
FPGA_BANK_PWR_B
PWR_ON_RST#
SYS_RST#
+FPGA_BANK_A
+FPGA_BANK_B
R1 0R R0402, 1%
ARM_PWR_ON_RST#
R2 0R R0402, 1%
ARM_SYS_RST#
U_USB_Micro_UART
USB_Micro_UART.SchDoc
USB_UART
USB_UART_TYPE-C
U_CED_Module_FPGA_ConnA
CED_Module_FPGA_Conn.SchDoc
FPGA_X
X_FPGA_X
PWR_GOOD
U_USB_TypeC_HardwareCTRL
USB_TypeC_HardwareCTRL.SchDoc
USB_UART_TYPE-C
R3 0R R0402, 1%
ARM_PWR_ON_RST#
R4 0R R0402, 1%
ARM_SYS_RST#
U_CED_Module_FPGA_ConnB
CED_Module_FPGA_Conn.SchDoc
R8 0R R0402, 1%
ARM_PWR_ON_RST#
R10 0R R0402, 1%
ARM_SYS_RST#
U_Power_Top
Power_Top.SchDoc
PWR_GOOD
DDRVREF
R5 1M R0402, 1%
R6 1M R0402, 1%
R7 1M R0402, 1%
R9 1M R0402, 1%
R11 1M R0402, 1%
R12 1M R0402, 1%
R13 1M R0402, 1%
H1 M3_MOUNTING_HOLE
H2 M3_MOUNTING_HOLE
H3 M3_MOUNTING_HOLE
H4 M3_MOUNTING_HOLE
H5 M3_MOUNTING_HOLE
H6 M3_MOUNTING_HOLE
H7 M3_MOUNTING_HOLE
SCRW1 M3 BLACK SCREW
SCRW2 M3 BLACK SCREW
SCRW3 M3 BLACK SCREW
SCRW4 M3 BLACK SCREW
SCRW5 M3 BLACK SCREW
SCRW6 M3 BLACK SCREW
SCRW7 M3 BLACK SCREW
GND
FID1 FIDUCIAL
FID2 FIDUCIAL
FID3 FIDUCIAL
FID4 FIDUCIAL
Title CED - Ocelot Project
Size: A3
Number: 1
Revision: A
Date: 2019-07-04
Time: 9:28:34 PM
Sheet1 of 20
File: G:\Shared drives\CED - Team Drive\Design - Engineering\CED Projects\Ocelot\Altium Project\REV A.00\CED_Zynq_7007S_Top_Sheet.SchDoc
Chester Electronic Design
Guelph, Ontario
Canada

<> Xilinx Part Library <>

XC7Z007S-CLG400 Does not exist in the Altium Xilinx Zynq-7000 Library. However XC7Z020-CLG400 is a Migration Path from XC7Z007S-CLG400. As XC7Z020-CLG400 exists in in the Altium Xilinx Zynq-7000 Library, that part has been selected as a Standin.



Title CED - Zynq 7007S Top			Chester Electronic Design Guelph, Ontario Canada
Size: A3	Number: 2	Revision: A	
Date: 2019-07-04	Time: 9:28:34 PM	Sheet 2 of 20	
File: G:\Shared drives\CED - Team Drive\Design - Engineering\CED Projects\Ocelot\Altium Project\REV A.00\Xilinx_Zynq-7007S-Top.SchDoc			



Title	CED - Zynq 7007S ARM		
Size: A3	Number: 3	Revision: A	Chester Electronic Design Guelph, Ontario Canada
Date: 2019-07-04	Time: 9:28:34 PM	Sheet3 of 20	
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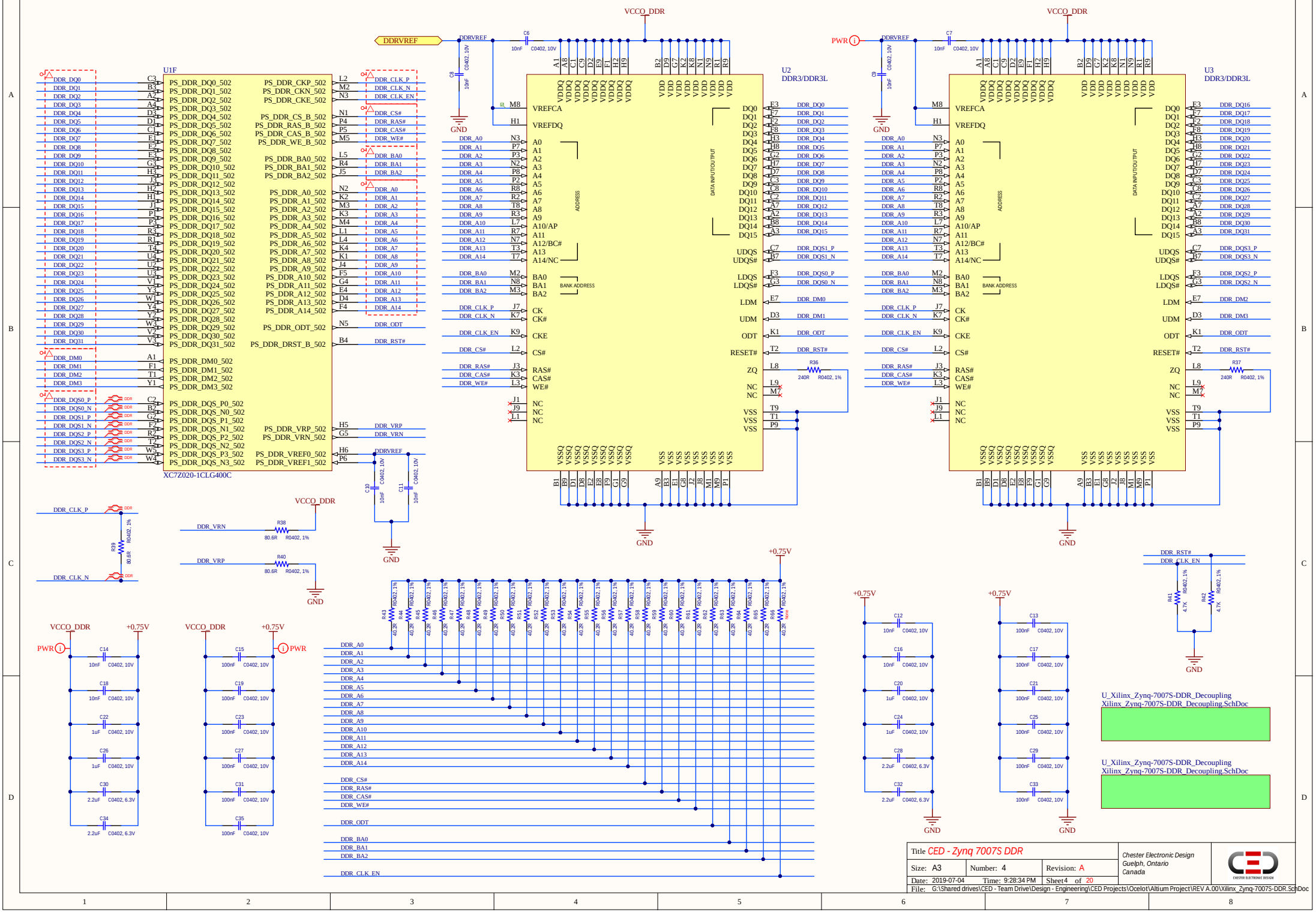
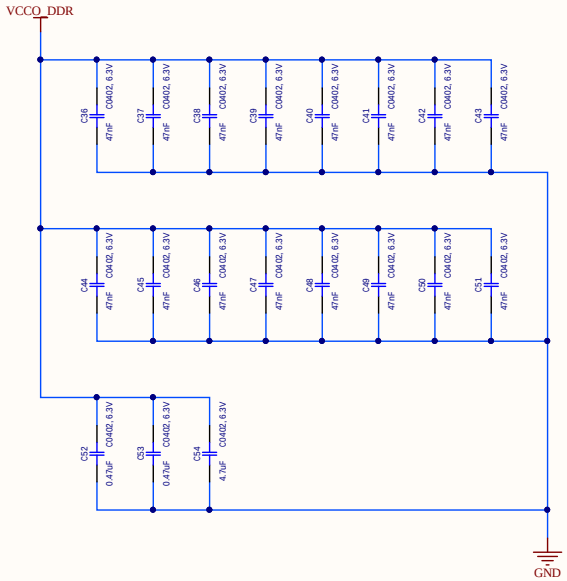
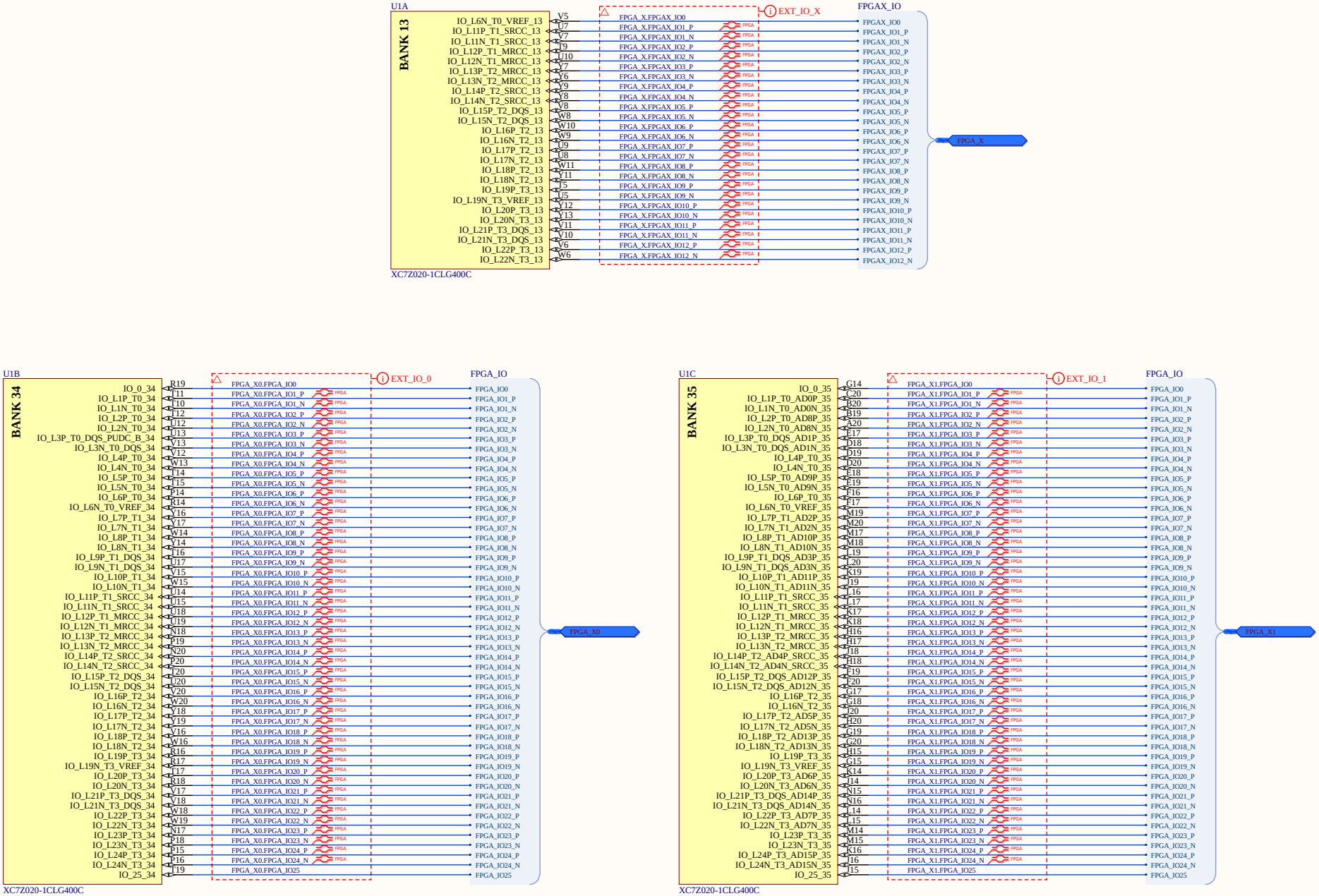

U1F
XC7Z020-1CLG400C
U2
DDR3/DDR3L
U3
DDR3/DDR3L
VCCO_DDR
DDRVREF
PWR
GND
+0.75V
VREFCA
VREFDQ
ADDRESS
BANK ADDRESS
DATA INPUT/OUTPUT
U_Xilinx_Zynq-7007S-DDR_Decoupling
Xilinx_Zynq-7007S-DDR_Decoupling.SchDoc
Title CED - Zynq 7007S DDR
Size: A3
Number: 4
Revision: A
Chester Electronic Design
Guelph, Ontario
Canada
Date: 2019-07-04
Time: 9:28:34 PM
Sheet4 of 20
File: G:\Shared drives\CED - Team Drive\Design - Engineering\CED Projects\Ocelot\Altium Project\REV A.00\Xilinx_Zynq-7007S-DDR.SchDoc



Title *CED - Zynq 7007S DDR Decoupling*			*Chester Electronic Design* *Guelph, Ontario* *Canada*
Size: A3	Number: 5	Revision: A	
Date: 2019-07-04	Time: 9:28:35 PM	Sheet5 of 20	
File: G:\Shared drives\CED - Team Drive\Design - Engineering\CED Projects\Ocelot\Altium Project\REV A.00\Xilinx_Zynq-7007S-DDR_Decoupling.Sch			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IO_L11P_T1_SRCC_13
IO_L11N_T1_SRCC_13
IO_L12P_T1_MRCC_13
IO_L12N_T1_MRCC_13
IO_L13P_T2_MRCC_13
IO_L13N_T2_MRCC_13
IO_L14P_T2_SRCC_13
IO_L14N_T2_SRCC_13
IO_L15P_T2_DQS_13
IO_L15N_T2_DQS_13
IO_L16P_T2_13
IO_L16N_T2_13
IO_L17P_T2_13
IO_L17N_T2_13
IO_L18P_T2_13
IO_L18N_T2_13
IO_L19P_T3_13
IO_L19N_T3_VREF_13
IO_L20P_T3_13
IO_L20N_T3_13
IO_L21P_T3_DQS_13
IO_L21N_T3_DQS_13
IO_L22P_T3_13
IO_L22N_T3_13
V5
U7
V7
T9
U10
T7
T6
Y9
Y8
V8
W8
W10
W9
U9
U8
W11
Y11
T5
U5
Y12
Y13
Y11
Y10
V6
W6
FPGA_X.FPGAX_IO0
FPGA_X.FPGAX_IO1_P
FPGA_X.FPGAX_IO1_N
FPGA_X.FPGAX_IO2_P
FPGA_X.FPGAX_IO2_N
FPGA_X.FPGAX_IO3_P
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FPGA_X.FPGAX_IO4_N
FPGA_X.FPGAX_IO5_P
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FPGA_X.FPGAX_IO6_N
FPGA_X.FPGAX_IO7_P
FPGA_X.FPGAX_IO7_N
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FPGA_X.FPGAX_IO8_N
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FPGAX_IO8_N
FPGAX_IO9_P
FPGAX_IO9_N
FPGAX_IO10_P
FPGAX_IO10_N
FPGAX_IO11_P
FPGAX_IO11_N
FPGAX_IO12_P
FPGAX_IO12_N
FPGA_X
XC7Z020-1CLG400C
U1B
BANK 34
IO_0_34
IO_L1P_T0_34
IO_L1N_T0_34
IO_L2P_T0_34
IO_L2N_T0_34
IO_L3P_T0_DQS_PUDC_B_34
IO_L3N_T0_DQS_34
IO_L4P_T0_34
IO_L4N_T0_34
IO_L5P_T0_34
IO_L5N_T0_34
IO_L6P_T0_34
IO_L6N_T0_VREF_34
IO_L7P_T1_34
IO_L7N_T1_34
IO_L8P_T1_34
IO_L8N_T1_34
IO_L9P_T1_DQS_34
IO_L9N_T1_DQS_34
IO_L10P_T1_34
IO_L10N_T1_34
IO_L11P_T1_SRCC_34
IO_L11N_T1_SRCC_34
IO_L12P_T1_MRCC_34
IO_L12N_T1_MRCC_34
IO_L13P_T2_MRCC_34
IO_L13N_T2_MRCC_34
IO_L14P_T2_SRCC_34
IO_L14N_T2_SRCC_34
IO_L15P_T2_DQS_34
IO_L15N_T2_DQS_34
IO_L16P_T2_34
IO_L16N_T2_34
IO_L17P_T2_34
IO_L17N_T2_34
IO_L18P_T2_34
IO_L18N_T2_34
IO_L19P_T3_34
IO_L19N_T3_VREF_34
IO_L20P_T3_34
IO_L20N_T3_34
IO_L21P_T3_DQS_34
IO_L21N_T3_DQS_34
IO_L22P_T3_34
IO_L22N_T3_34
IO_L23P_T3_34
IO_L23N_T3_34
IO_L24P_T3_34
IO_L24N_T3_34
IO_25_34
R19
L11
L10
L12
U12
U13
V13
V12
W13
L14
L15
P14
R14
Y16
Y17
W14
Y14
L16
U17
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U15
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U19
N18
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Y19
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W16
R16
R17
U17
R18
V17
V18
W18
W19
N17
P18
P15
P16
T19
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FPGA_X0.FPGA_IO2_P
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FPGA_IO25
FPGA_X0
XC7Z020-1CLG400C
U1C
BANK 35
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IO_L1N_T0_AD0N_35
IO_L2P_T0_AD8P_35
IO_L2N_T0_AD8N_35
IO_L3P_T0_DQS_AD1P_35
IO_L3N_T0_DQS_AD1N_35
IO_L4P_T0_35
IO_L4N_T0_35
IO_L5P_T0_AD9P_35
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IO_L20N_T3_AD6N_35
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C16.FPGA_X1.FPGA_IO6_P
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H17.FPGA_X1.FPGA_IO13_N
J18.FPGA_X1.FPGA_IO14_P
H18.FPGA_X1.FPGA_IO14_N
J19.FPGA_X1.FPGA_IO15_P
J20.FPGA_X1.FPGA_IO15_N
G17.FPGA_X1.FPGA_IO16_P
G18.FPGA_X1.FPGA_IO16_N
J20.FPGA_X1.FPGA_IO17_P
H20.FPGA_X1.FPGA_IO17_N
G19.FPGA_X1.FPGA_IO18_P
G20.FPGA_X1.FPGA_IO18_N
H15.FPGA_X1.FPGA_IO19_P
G15.FPGA_X1.FPGA_IO19_N
K14.FPGA_X1.FPGA_IO20_P
J14.FPGA_X1.FPGA_IO20_N
N15.FPGA_X1.FPGA_IO21_P
N16.FPGA_X1.FPGA_IO21_N
L14.FPGA_X1.FPGA_IO22_P
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FPGA_IO
FPGA_IO0
FPGA_IO1_P
FPGA_IO1_N
FPGA_IO2_P
FPGA_IO2_N
FPGA_IO3_P
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FPGA_IO23_P
FPGA_IO23_N
FPGA_IO24_P
FPGA_IO24_N
FPGA_IO25
FPGA_X1
XC7Z020-1CLG400C
Title CED - Zynq 7007S FPGA
Size: A3
Number: 6
Revision: A
Date: 2019-07-04
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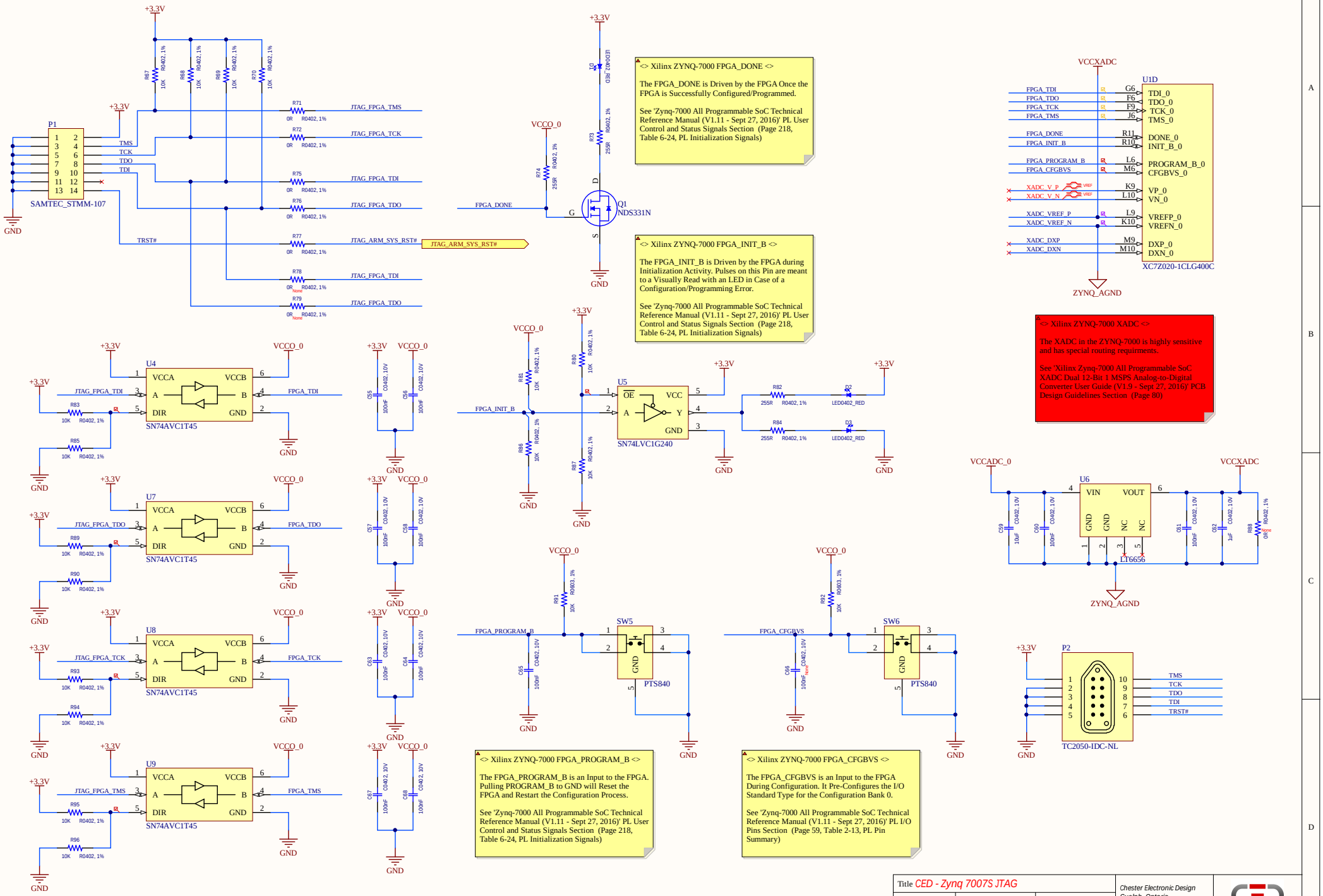
File: G:\Shared drives\CED - Team Drive\Design - Engineering\CED Projects\Ocelot\Altium Project\REV A.00\Xilinx_Zynq-7007S-FPGA.SchDoc
Chester Electronic Design
Guelph, Ontario
Canada


P1
SAMTEC_STMM-107
TMS
TCK
TDO
TDI
TRST#
JTAG_FPGA_TMS
JTAG_FPGA_TCK
JTAG_FPGA_TDI
JTAG_FPGA_TDO
JTAG_ARM_SYS_RST#
FPGA_DONE
Q1
NDS331N
<> Xilinx ZYNQ-7000 FPGA_DONE <>
The FPGA_DONE is Driven by the FPGA Once the FPGA is Successfully Configured/Programmed.
See 'Zynq-7000 All Programmable SoC Technical Reference Manual (V1.11 - Sept 27, 2016)' PL User Control and Status Signals Section (Page 218, Table 6-24, PL Initialization Signals)
<> Xilinx ZYNQ-7000 FPGA_INIT_B <>
The FPGA_INIT_B is Driven by the FPGA during Initialization Activity. Pulses on this Pin are meant to a Visually Read with an LED in Case of a Configuration/Programming Error.
See 'Zynq-7000 All Programmable SoC Technical Reference Manual (V1.11 - Sept 27, 2016)' PL User Control and Status Signals Section (Page 218, Table 6-24, PL Initialization Signals)
U1D
XC7Z020-1CLG400C
FPGA_TDI
FPGA_TDO
FPGA_TCK
FPGA_TMS
FPGA_DONE
FPGA_INIT_B
FPGA_PROGRAM_B
FPGA_CFGBVS
XADC_V_P
XADC_V_N
XADC_VREF_P
XADC_VREF_N
XADC_DXP
XADC_DXN
ZYNQ_AGND
<> Xilinx ZYNQ-7000 XADC <>
The XADC in the ZYNQ-7000 is highly sensitive and has special routing requirments.
See 'Xilinx Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide (V1.9 - Sept 27, 2016)' PCB Design Guidelines Section (Page 80)
U4
U7
U8
U9
SN74AVC1T45
U5
SN74LVC1G240
U6
LT6656
SW5
SW6
PTS840
P2
TC2050-IDC-NL
<> Xilinx ZYNQ-7000 FPGA_PROGRAM_B <>
The FPGA_PROGRAM_B is an Input to the FPGA. Pulling PROGRAM_B to GND will Reset the FPGA and Restart the Configuration Process.
See 'Zynq-7000 All Programmable SoC Technical Reference Manual (V1.11 - Sept 27, 2016)' PL User Control and Status Signals Section (Page 218, Table 6-24, PL Initialization Signals)
<> Xilinx ZYNQ-7000 FPGA_CFGBVS <>
The FPGA_CFGBVS is an Input to the FPGA During Configuration. It Pre-Configures the I/O Standard Type for the Configuration Bank 0.
See 'Zynq-7000 All Programmable SoC Technical Reference Manual (V1.11 - Sept 27, 2016)' PL I/O Pins Section (Page 59, Table 2-13, PL Pin Summary)
Title CED - Zynq 7007S JTAG
Size: A3
Number: 7
Revision: A
Date: 2019-07-04
Time: 9:28:35 PM
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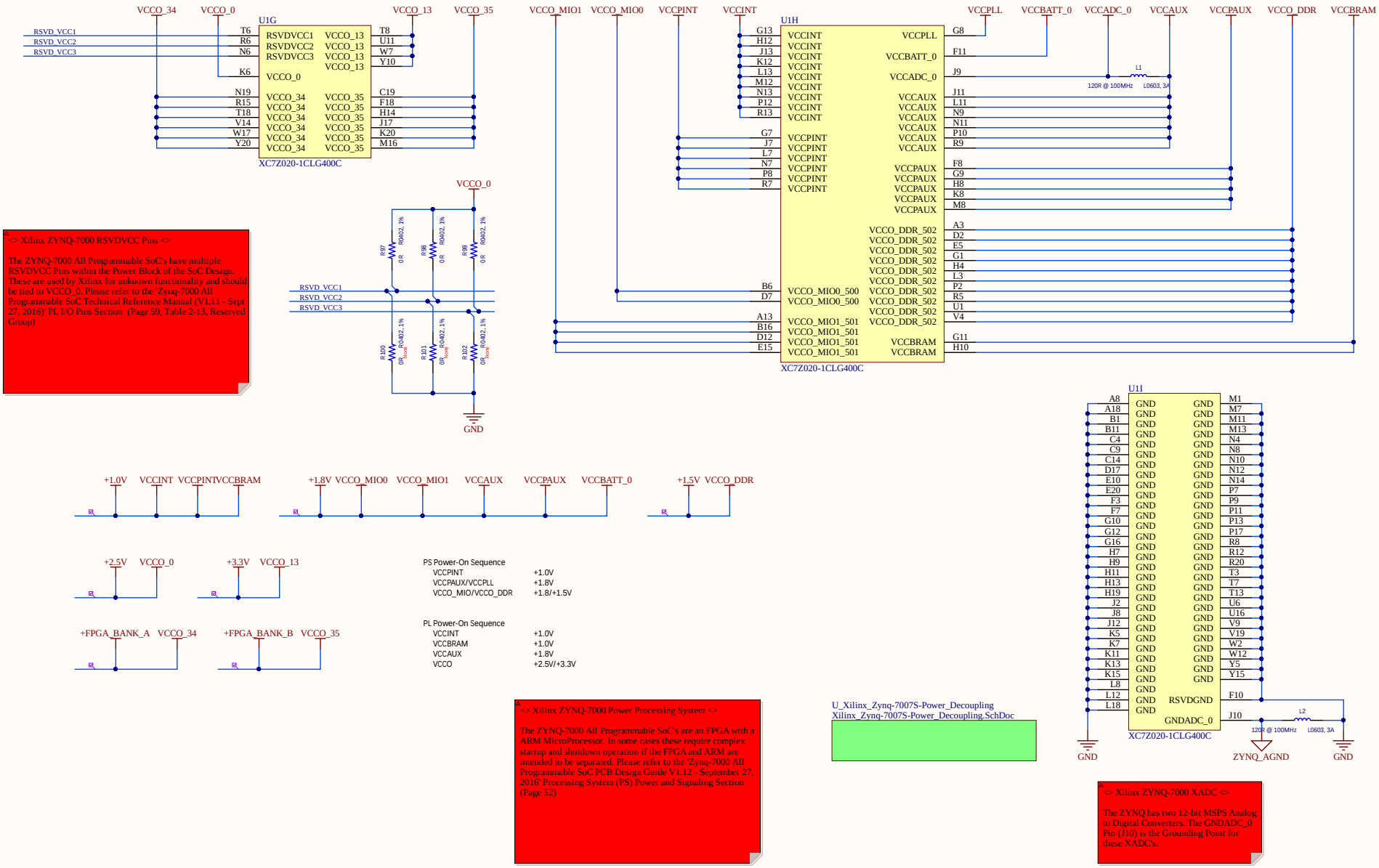
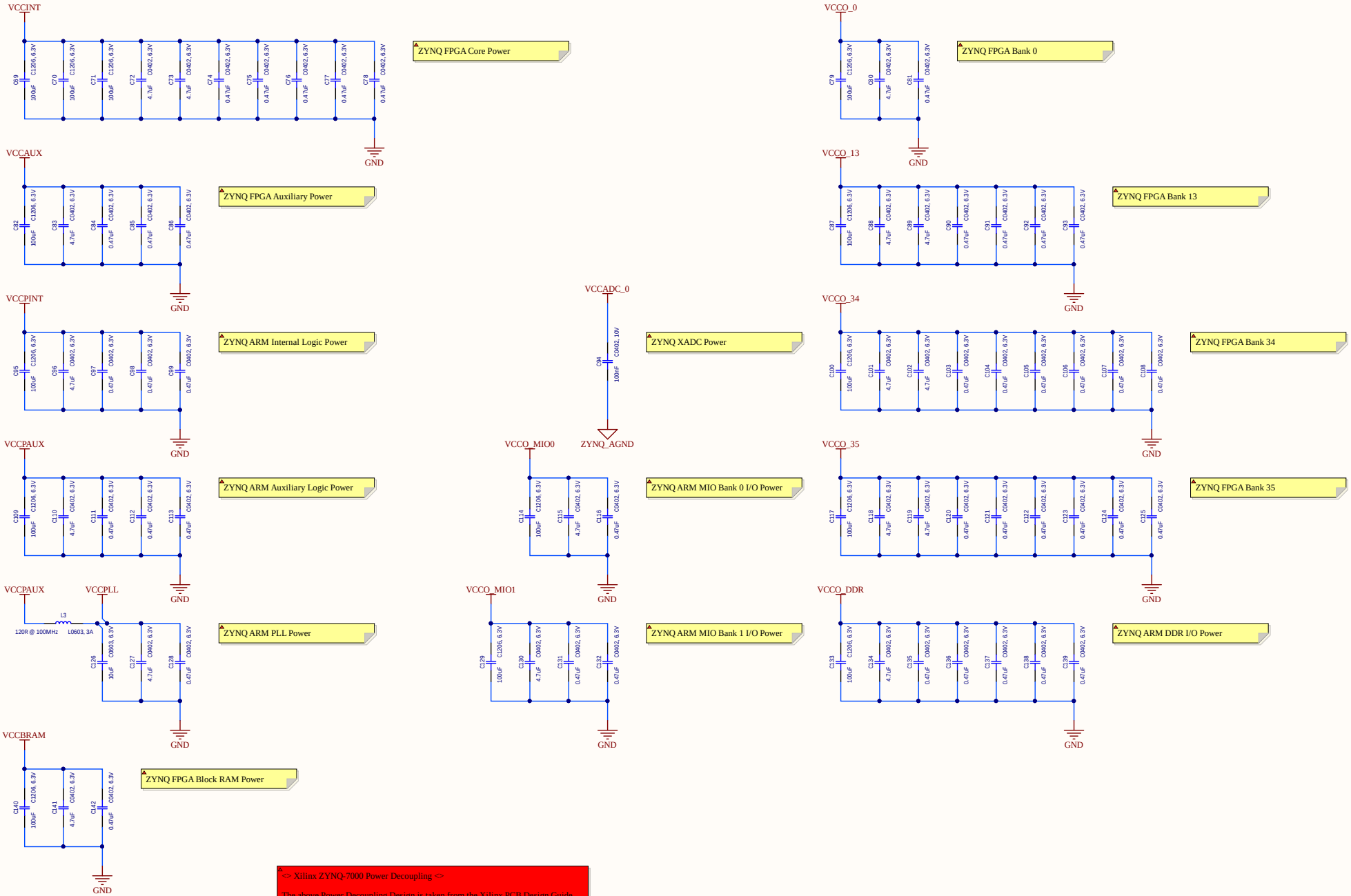
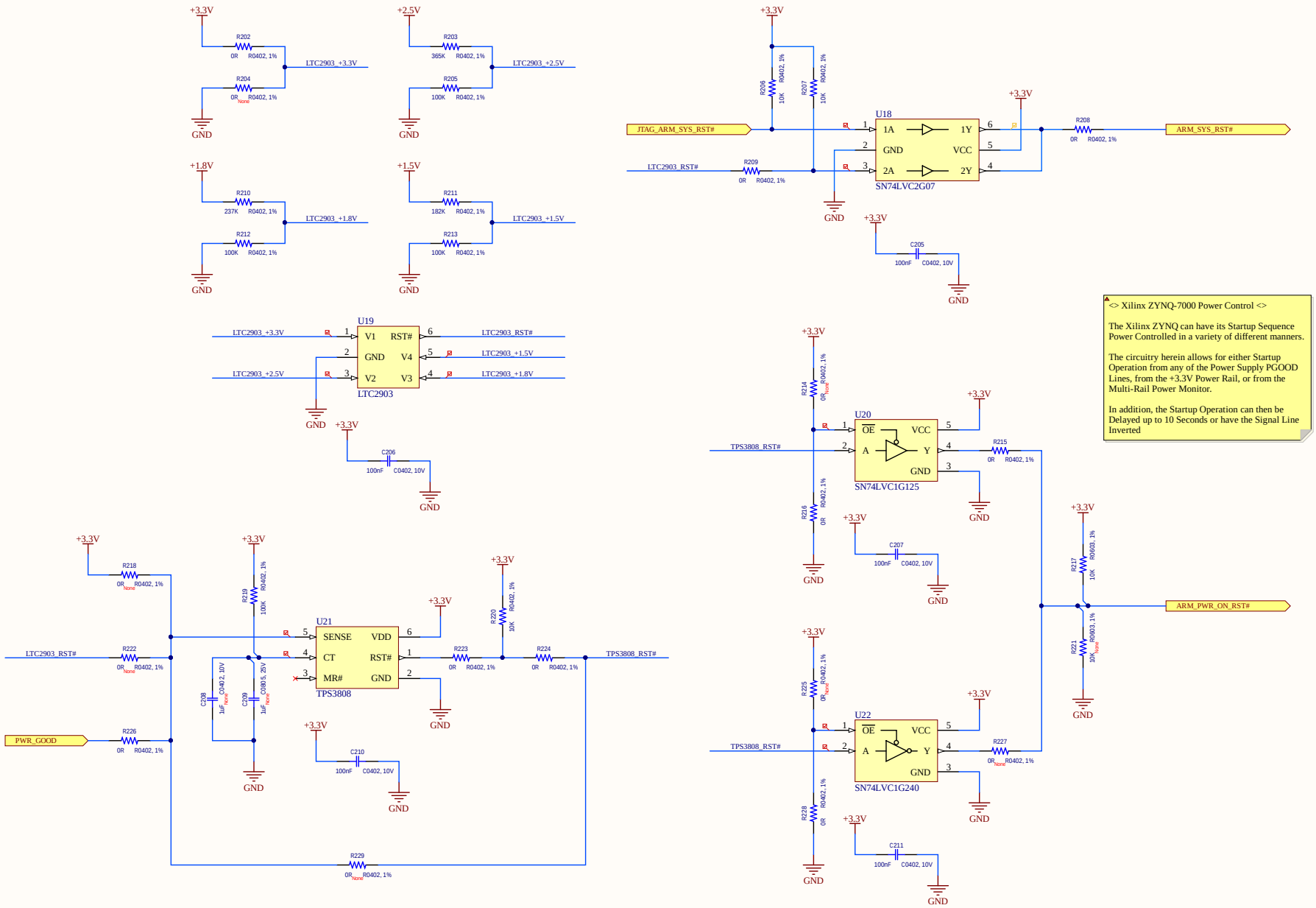
File: G:\Shared drives\CED - Team Drive\Design - Engineering\CED Projects\Ocelot\Altium Project\REV A.00\Xilinx_Zynq-7007S-JTAG.SchDoc
Chester Electronic Design
Guelph, Ontario
Canada



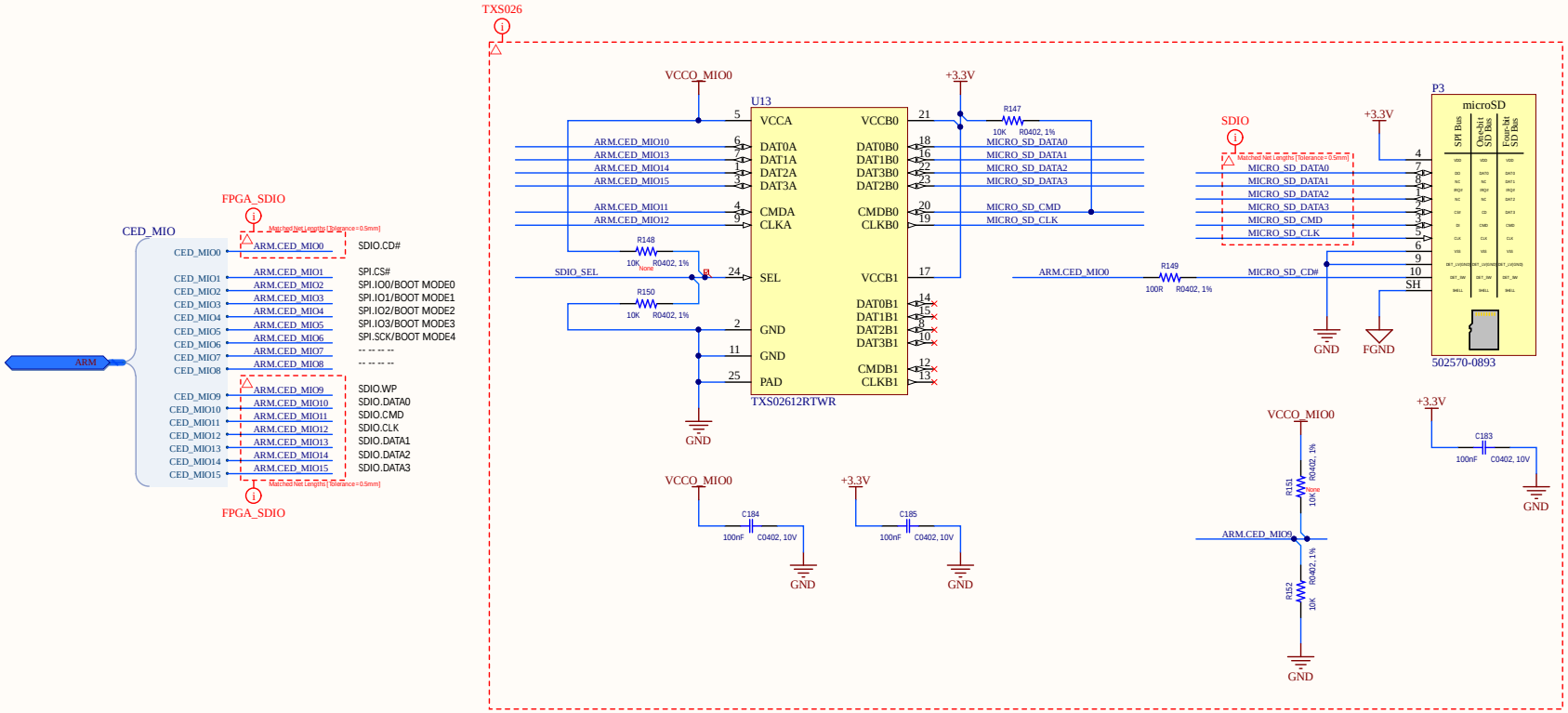
Title	CED - Zynq 7007S Power Top		Chester Electronic Design Guelph, Ontario Canada
Size: A3	Number: 8	Revision: A	
Date: 2019-07-04	Time: 9:28:35 PM	Sheet 8 of 20	
File: G:\Shared drives\CED - Team Drive\Design - Engineering\CED Projects\Ocelot\Altium Project\REV A.00\Xilinx_Zynq-7007S-Power.SchDoc			



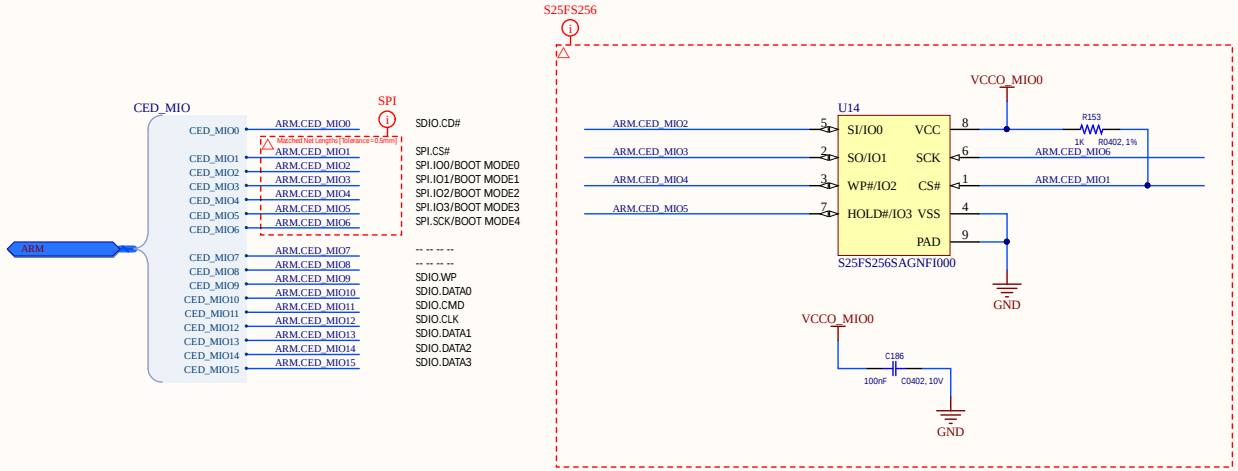
Title	CED - Zynq 7007S Power Decoupling		Chester Electronic Design Guelph, Ontario Canada
Size: A3	Number: 9	Revision: A	
Date: 2019-07-04	Time: 9:28:36 PM	Sheet 9 of 20	
File: G:\Shared drives\CED - Team Drive\Design - Engineering\CED Projects\Ocelot\Altium Project\REV A.00\Xilinx_Zynq-7007S-Power_Decoupling.SchDoc			



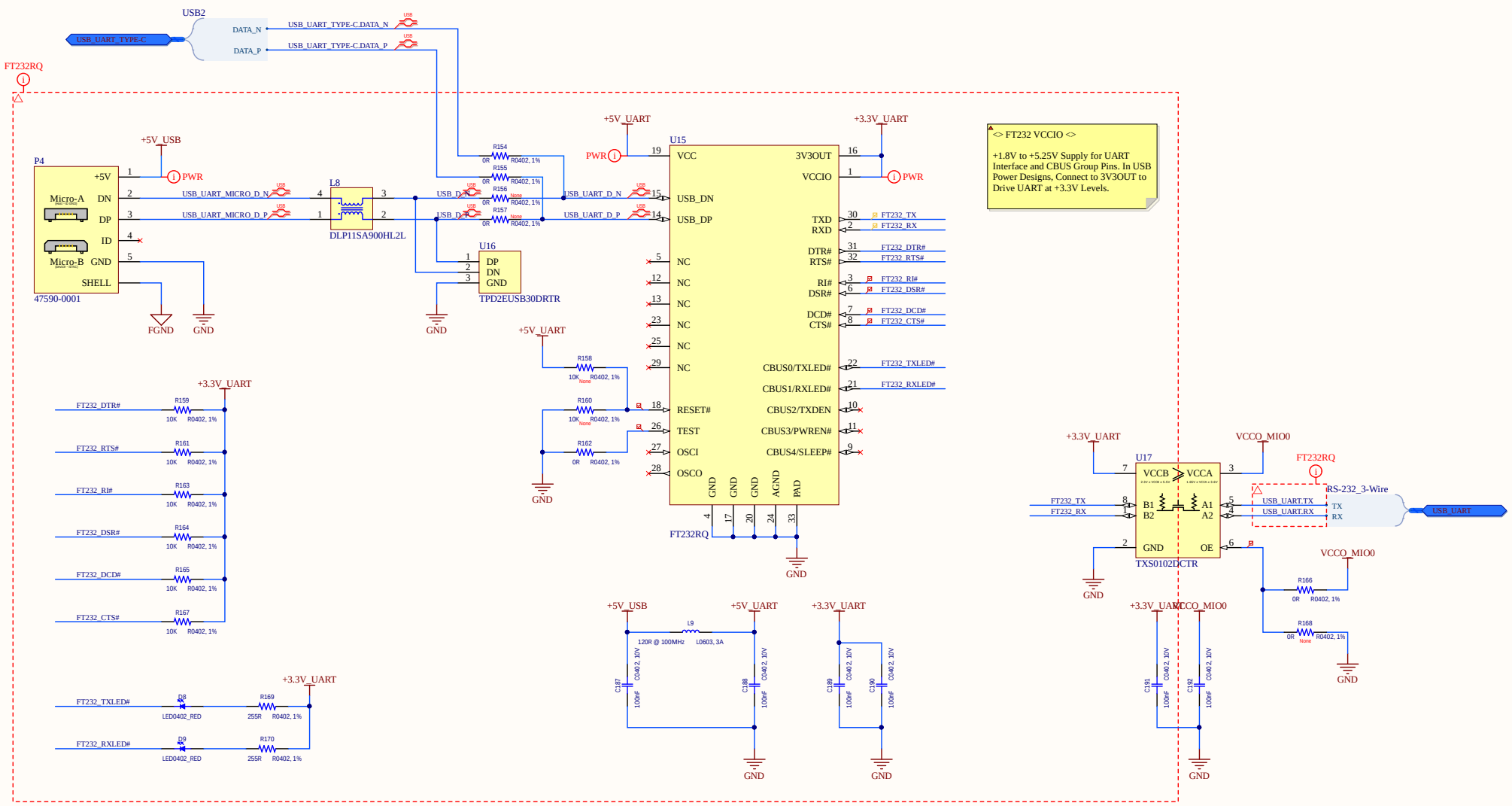
Title	CED - Zynq 7007S Power Control		Chester Electronic Design Guelph, Ontario Canada
Size: A3	Number: 10	Revision: A	
Date: 2019-07-04	Time: 9:28:36 PM	Sheet 10 of 20	
File: G:\Shared drives\CED - Team Drive\Design - Engineering\CED Projects\Ocelot\Altium Project\REV A.00\Power_Control.SchDoc			



Title	CED - Micro SD		
Size: A3	Number: 11	Revision: A	Chester Electronic Design Guelph, Ontario Canada
Date: 2019-07-04	Time: 9:28:36 PM	Sheet 11 of 20	
File: G:\Shared drives\CED - Team Drive\Design - Engineering\CED Projects\Ocelot\Altium Project\REV A.00\Storage_microSD.SchDoc			



Title	CED - SPI Flash		Chester Electronic Design Guelph, Ontario Canada
Size: A3	Number: 12	Revision: A	
Date: 2019-07-04	Time: 9:28:36 PM	Sheet 12 of 20	
File: G:\Shared drives\CED - Team Drive\Design - Engineering\CED Projects\Ocelot\Altium Project\REV A.00\Storage_SPI_Flash.SchDoc			



Title	CED - Micro USB UART		
Size: A3	Number: 13	Revision: A	
Date: 2019-07-04	Time: 9:28:36 PM	Sheet13 of 20	
File: G:\Shared drives\CED - Team Drive\Design - Engineering\CED Projects\Ocelot\Altium Project\REV A.00\USB_Micro_UART.SchDoc			

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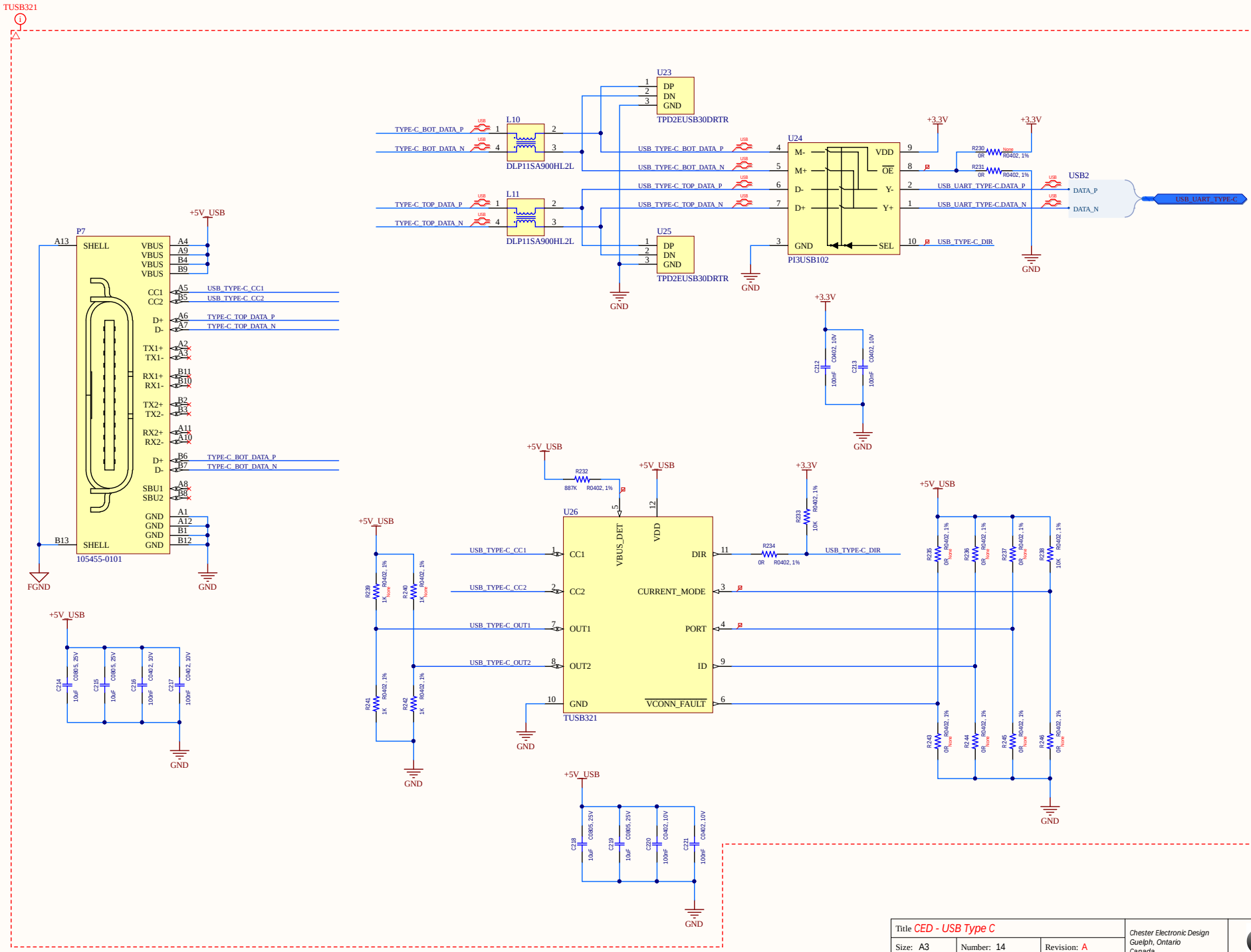
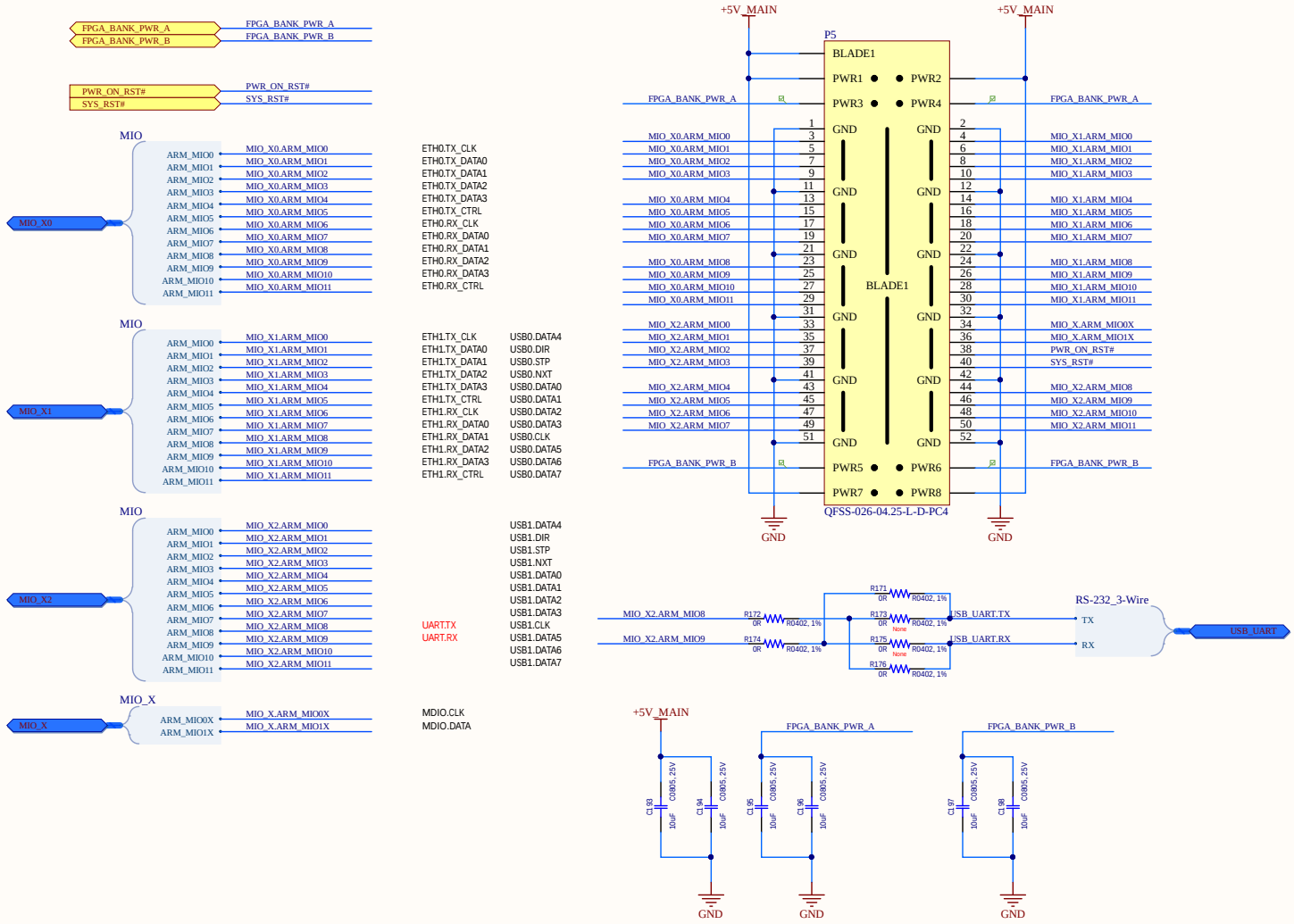
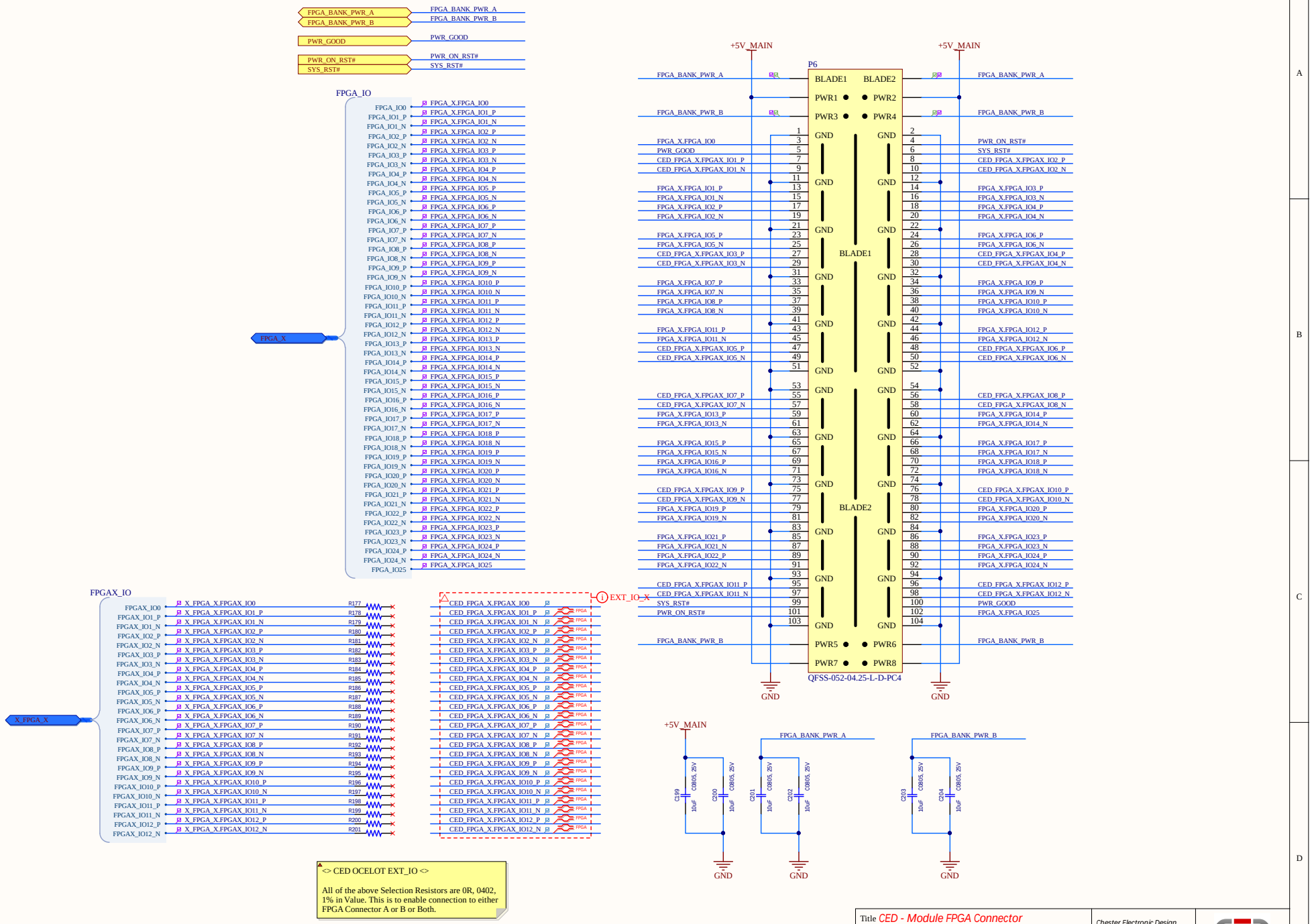


Title	CED - USB Type C		Chester Electronic Design Guelph, Ontario Canada
Size: A3	Number: 14	Revision: A	
Date: 2019-07-04	Time: 9:28:36 PM	Sheet14 of 20	
File: G:\Shared drives\CED - Team Drive\Design - Engineering\CED Projects\Ocelot\Altium Project\REV A.00\USB_TypeC_HardwareCTRL.SchDoc			



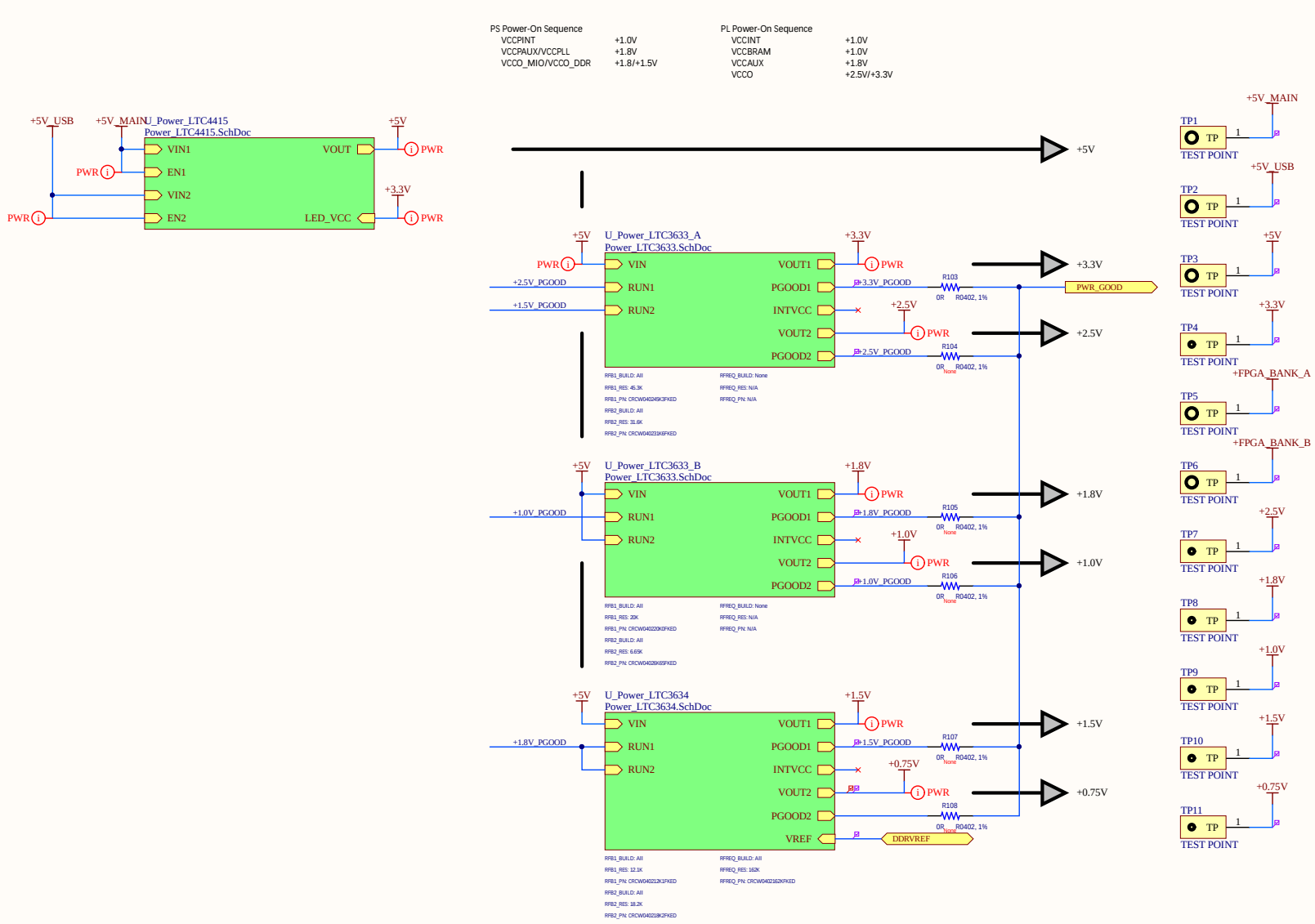
Title	CED - Module ARM Connector		Chester Electronic Design Guelph, Ontario Canada
Size: A3	Number: 15	Revision: A	
Date: 2019-07-04	Time: 9:28:36 PM	Sheet 15 of 20	
File: G:\Shared drives\CED - Team Drive\Design - Engineering\CED Projects\Ocelot\Altium Project\REV A.00\CED_Module_ARM_Conn.SchDoc			



<> CED OCELOT EXT_IO <>

All of the above Selection Resistors are 0R, 0402, 1% in Value. This is to enable connection to either FPGA Connector A or B or Both.

Title	CED - Module FPGA Connector		Chester Electronic Design Guelph, Ontario Canada
Size: A3	Number: 16	Revision: A	
Date: 2019-07-04	Time: 9:28:36 PM	Sheet 16 of 20	
File: G:\Shared drives\CED - Team Drive\Design - Engineering\CED Projects\Ocelot\Altium Project\REV A.00\CED_Module_FPGA_Conn.SchDoc			



Title	CED - Power Top		
Size: A3	Number: 17	Revision: A	
Date: 2019-07-04	Time: 9:28:37 PM	Sheet 17 of 20	
File: G:\Shared drives\CED - Team Drive\Design - Engineering\CED Projects\Ocelot\Altium Project\REV A.00\Power_Top.SchDoc			

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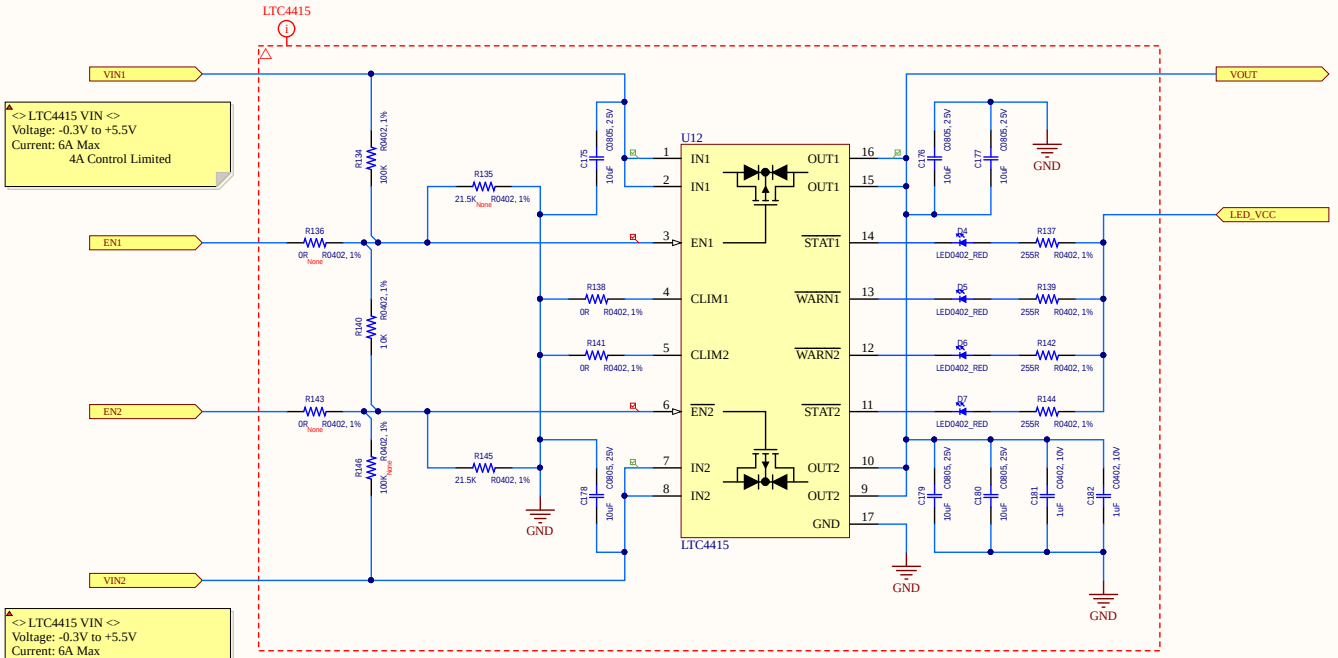


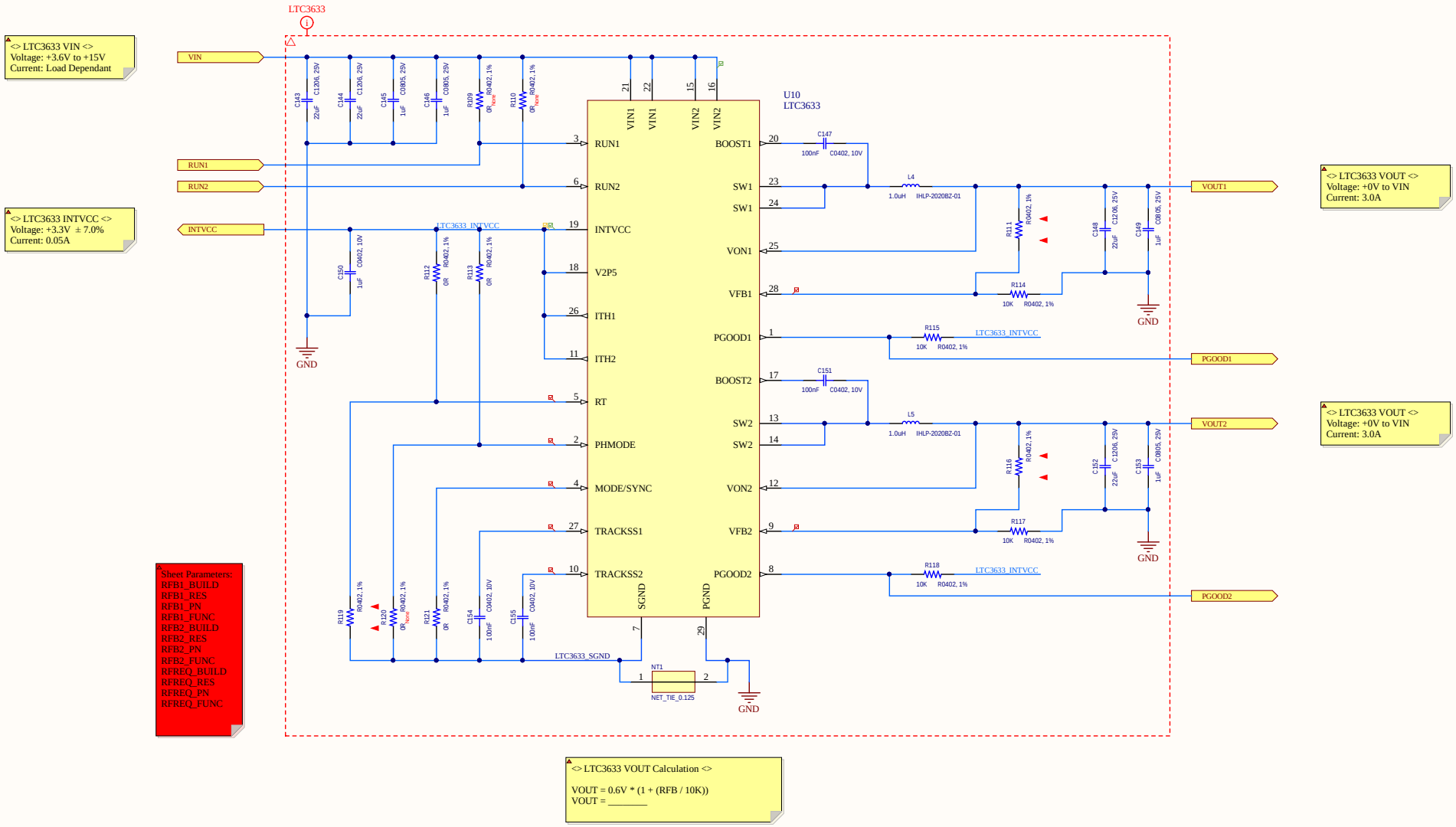
<> LTC4415 Prioritized Switchover Calculations <>

Power IN/OUT 2 Enable Switchover
VIN1 < 0.8V * (1 + ((R1 + R2) / R3))
VIN1 < 0.8V * (1 + ((100 + 10) / 21.5))
VIN1 < 4.893V

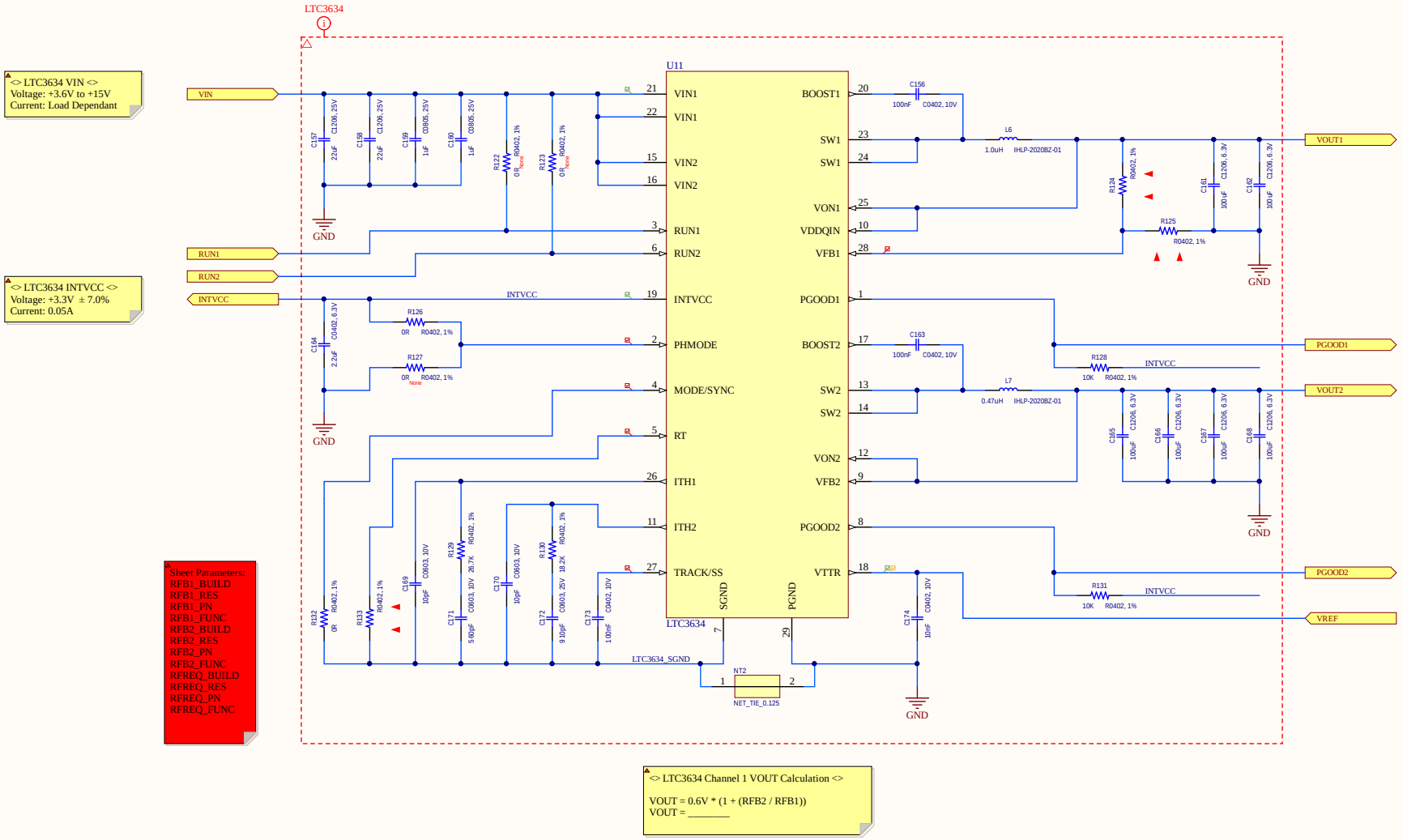
Power IN/OUT 2 Disable Switchover
VIN1 < (0.8V - VENHYST) * (1 + (R1 / (R2 + R3)))
VIN1 < (0.8V - 0.055V) * (1 + (100 / (10 + 21.5)))
VIN1 < 3.110V

Power Overlap
VOVERLAP ≈ VENTH * (R2 / R3)
VOVERLAP ≈ 0.8V * (10 / 21.5)
VOVERLAP ≈ 0.372V

Title CED - Power LTC4415			Chester Electronic Design Guelph, Ontario Canada
Size: A3	Number: 18	Revision: A	
Date: 2019-07-04	Time: 9:28:37 PM	Sheet 18 of 20	
File: G:\Shared drives\CED - Team Drive\Design - Engineering\CED Projects\Ocelot\Altium Project\REV A.00\Power_LTC4415.SchDoc			



Title CED - Power LTC3633			Chester Electronic Design Guelph, Ontario Canada
Size: A3	Number: 19	Revision: A	
Date: 2019-07-04	Time: 9:28:37 PM	Sheet 19 of 20	
File: G:\Shared drives\CED - Team Drive\Design - Engineering\CED Projects\Ocelot\Altium Project\REV A.00\Power_LTC3633.SchDoc			



Title CED - Power LTC3634			Chester Electronic Design Guelph, Ontario Canada
Size: A3	Number: 20	Revision: A	
Date: 2019-07-04	Time: 9:28:37 PM	Sheet 20 of 20	
File: G:\Shared drives\CED - Team Drive\Design - Engineering\CED Projects\Ocelot\Altium Project\REV A.00\Power_LTC3634.SchDoc			